MIT Splash 2021

Transistors!

Class Notes

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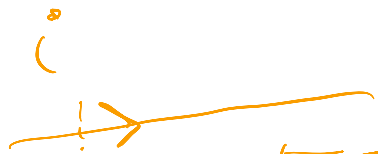
Voltage

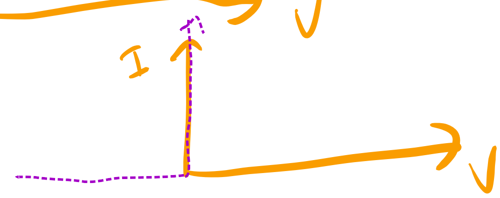
"push" on electrons

Current

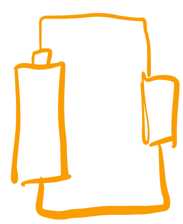


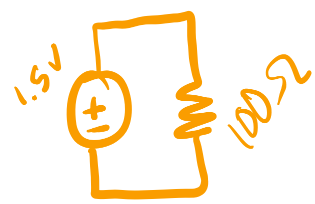
$5A = \frac{5C}{s}$

V-I Relations



Circuits





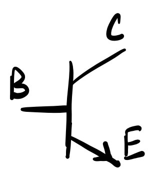
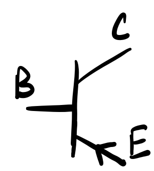
Ω

Schematics

- Two common types of transistors: MOSFETS and BJTs. We'll only consider BJTs in this class.
- Physics of how transistors work is beyond the scope of this class. Email us after if you want to learn about transistor physics!

BJTs (bipolar junction transistors)

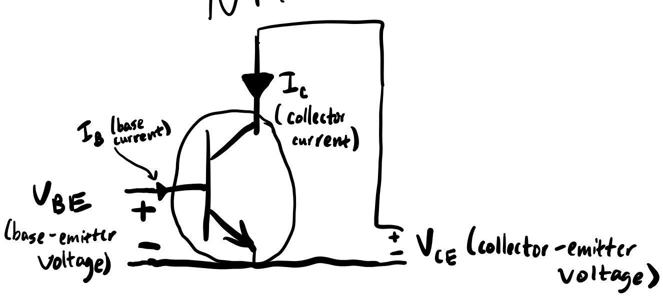
Two types: NPN and PNP. Type determined by chemical composition.

NPN	PNP
Schematic symbol: 	Schematic symbol: 

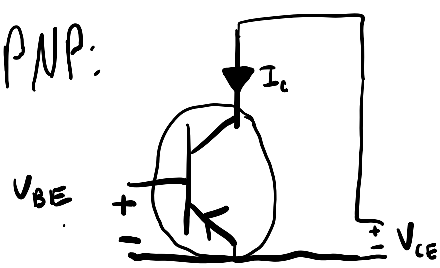
(b = base, c = collector, e = emitter)

Important values: V_{BE}, V_{CE}, I_c

NPN:

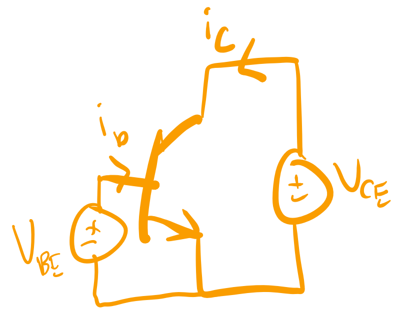


PNP:

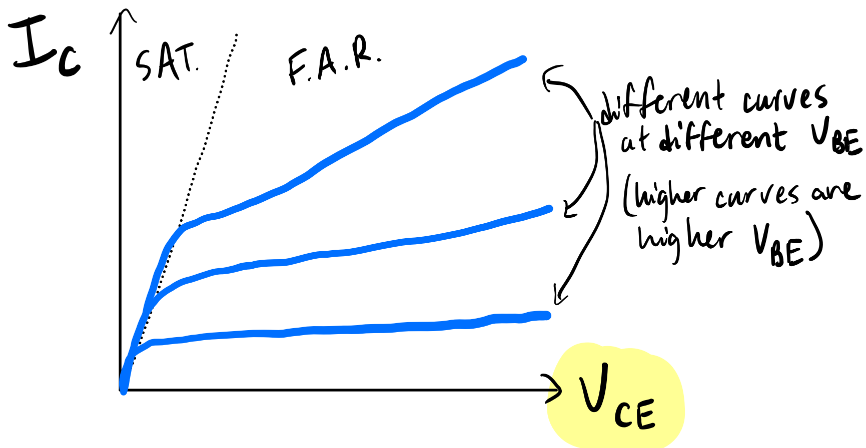


For PNP, usually V_{BE}, V_{CE}, and I_c are negative.

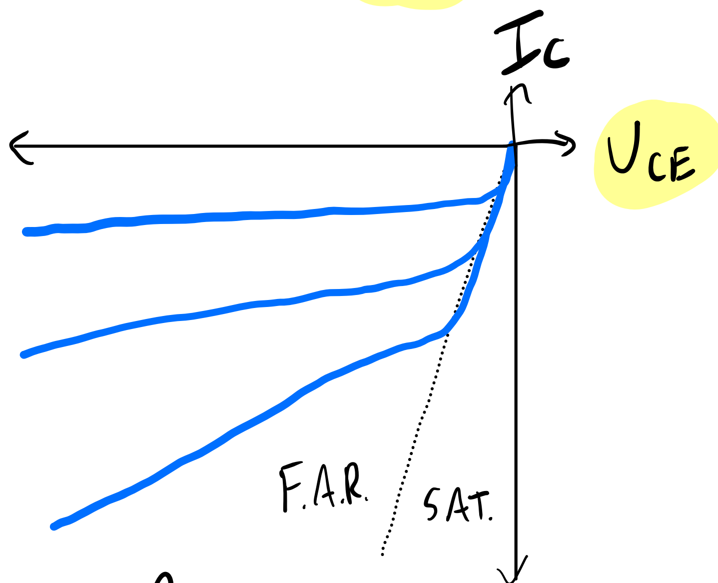
Modes of operation
(plots of I_C vs V_{CE})



NPN:



PNP:



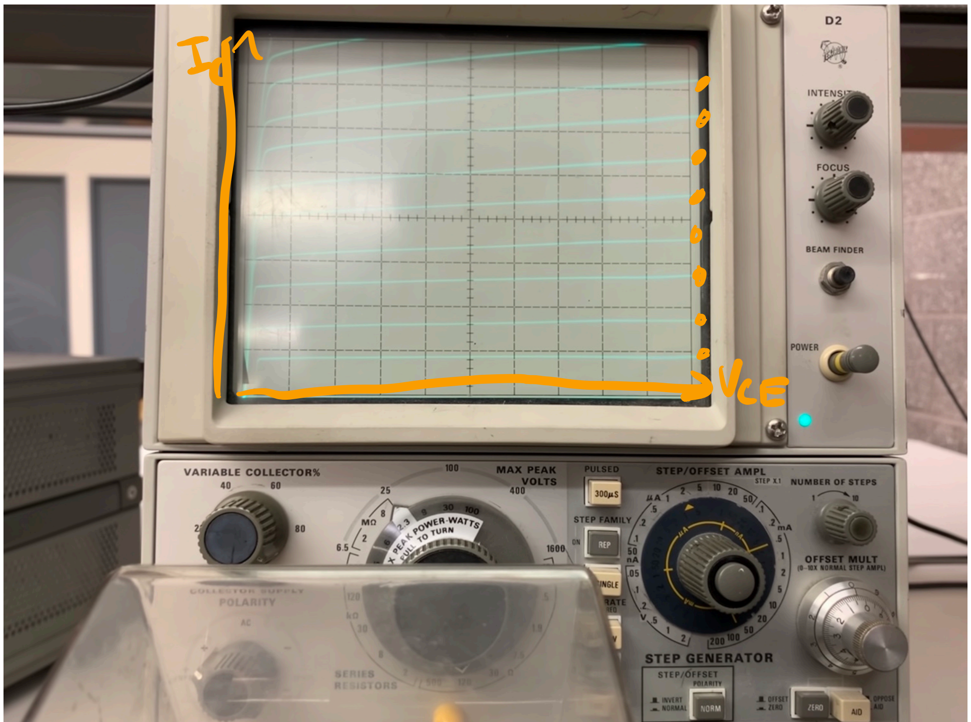
SAT: Saturation Region

F.A.R: Forward Active Region

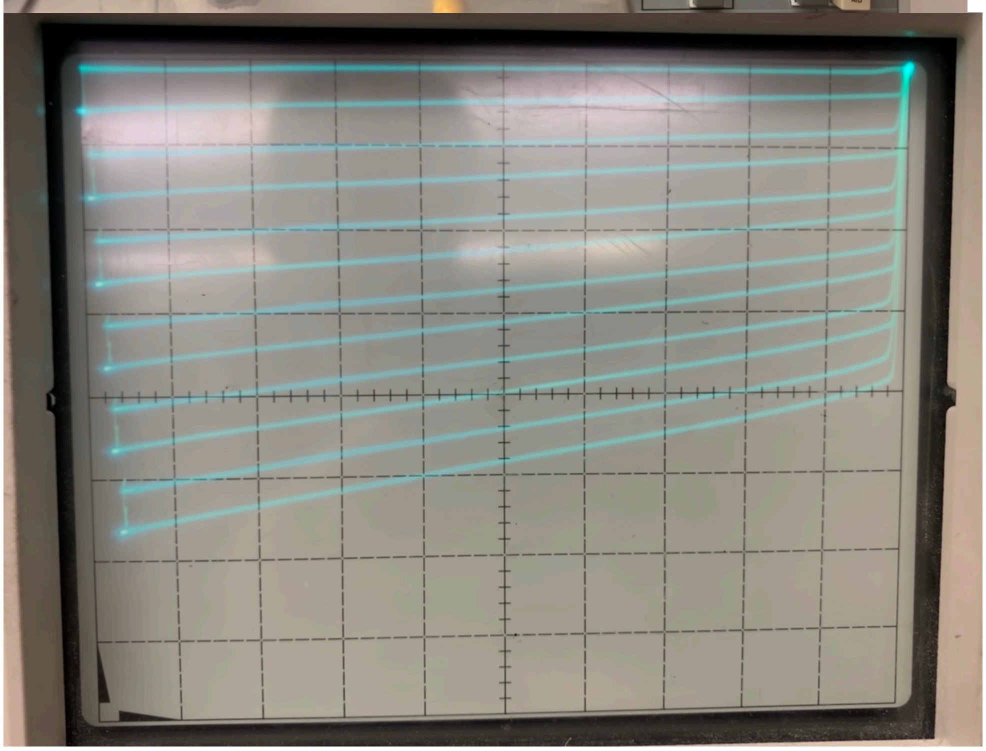
We'll only consider F.A.R. in this class.

I_C vs. V_{CE} measured on actual transistors:

NPN:



PNP:



(I took these measurements on a Tektronix 577 curve tracer in Nov. 2019)

In F.A.R.:

$$I_c = I_s e^{V_{BE}/V_{th}} \left(1 + \frac{V_{CE}}{V_A}\right)$$

(NPN)

Euler's constant (2.718...)

Base-Emitter voltage

Collector current

"Saturation current" (based on device dimensions and chemistry; typically near 1 fA (10^{-15} A).)

"Thermal voltage"

$$V_{th} = \frac{K_B T}{q}$$

K_B: Boltzmann's constant; T: Temperature (K); q: charge of electron

At room temp., $V_{th} \approx 25\,mV$.

"Early voltage" (named after James Early). Often, $V_{CE} \ll V_A$ (so $1 + \frac{V_{CE}}{V_A} \approx 1$) so we sometimes can ignore this term.

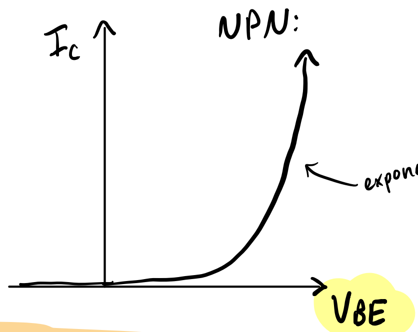
And $I_C = \beta_0 I_b$ for some constant β_0 ("current gain").

(Often, β is in the range 10 to 1000. We sometimes assume $I_B = 0$, since I_B is sometimes too small to affect the circuit if β is very high.)

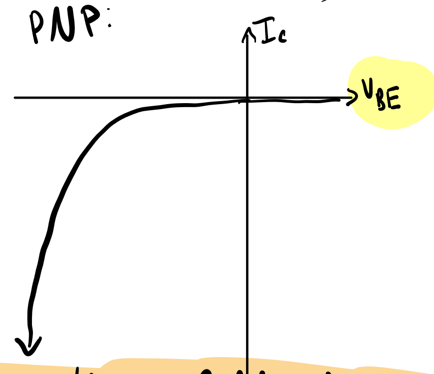
For PNP, $I_C = I_S e^{-V_{BE}/V_{th}} \left(1 + \frac{V_{CE}}{V_A}\right)$ (and I_S and V_A are negative).

Plots (at constant V_{CE}; V_{CE} is high enough that BJTs are in F.A.R.)

NPN:



PNP:



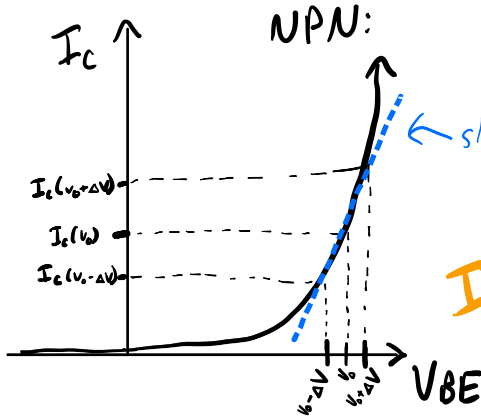
In this class, we'll consider NPN only

(but PNP operates the same way, just with some negative signs)

Small-Signal Parameters

What if we keep V_{BE} close to some constant value?

NPN:



← slope = $g_m = \frac{\partial I_c}{\partial V_{BE}}\Big|_{V_0}$

$I_c(v_0+v_{in}) = I_c(v_0) + g_m v_{in}$

($v_{in} < \Delta V$)

Then the I_c vs. V_{BE} curve is nearly linear!

We say its slope is g_m (transconductance).

$$g_m = \frac{\partial I_c}{\partial V_{BE}}\Big|_{V_0} = \frac{\partial}{\partial V_{BE}} I_s e^{V_{BE}/V_{th}}\Big|_{V_0}$$ (ignore Early effect)

$\left(=\frac{1}{\Omega}\right)$

$$= \boxed{\frac{I_s}{V_{th}} e^{V_0/V_{th}}} = \boxed{\frac{I_c(v_0)}{V_{th}}}$$

@1mA $g_m = \frac{1}{25\,\Omega}$

(where $I_c(v_0)$ is the current I_c when $V_{BE} = V_0$; it's not $I_c \times V_0$).

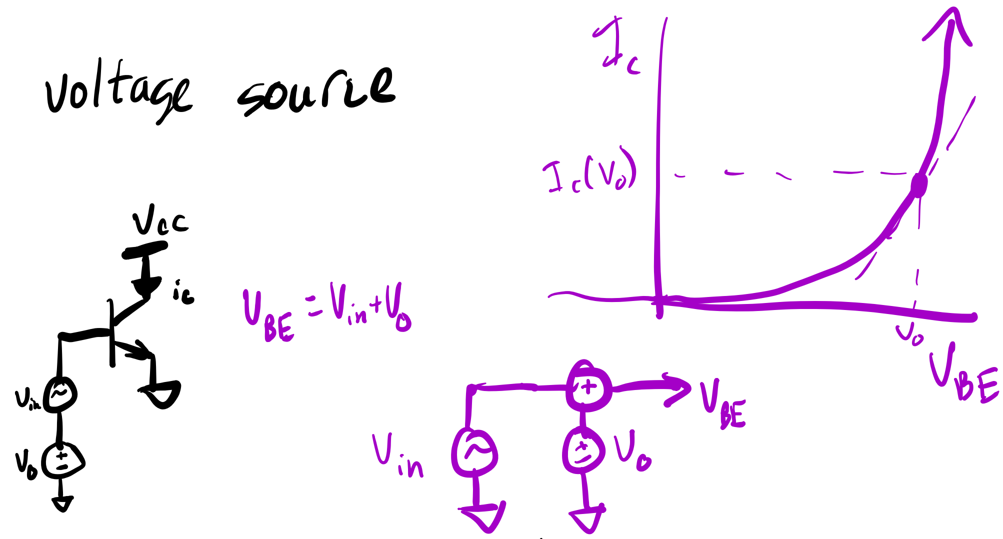
This linear behavior makes analysis easier!

We call the set of parameters around which we linearize (like V_0, I_c, etc.) the **operating point**.

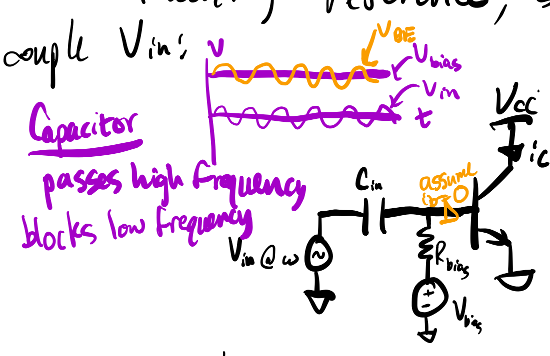
But how to make V_{BE} stay in a small range around some V_0 so we can analyze linearly? And how to set this V_0?

We call techniques for this <u>biasing</u>.

One way: voltage source



But it's hard to implement a voltage source with a floating reference, so we can capacitatively couple V_{in}:



Exercise for reader: why do we need R_{bias}? why can't we directly connect V_{bias} to the base? Think about it now; we'll answer it soon.

Capacitative coupling only works for AC input signals, so it's not uniformly applicable. But it's a simple solution, so it's often used.

Let's compute V_{BE} in the capacitatively coupled case:

Assume $I_b = 0$.

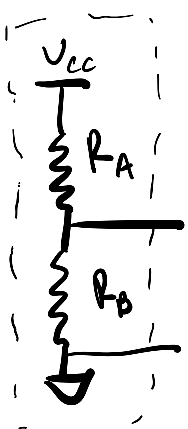
$$V_{BE} = V_{Bias} + V_{in}\left(\frac{R_{bias}}{R_{bias} + jX_{C_{in}}}\right) = V_{bias} + V_{in}\left(\frac{R_{Bias}}{R_{bias} + \frac{1}{j\omega C_{in}}}\right)$$

Then if $R_{bias} \gg \frac{1}{\omega C_{in}}$ (input freq. / input capacitance) (i.e. frequency is sufficiently high), $V_{BE} \approx V_{bias} + V_{in}$, as desired.

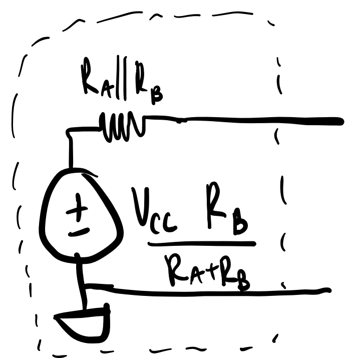
How to generate V_{bias}?

Typically with a voltage divider from VCC to ground:

$$R_A \| R_B = \frac{1}{\frac{1}{R_A} + \frac{1}{R_B}}$$



Thevenin eq.



A voltage source with resistor, like we want!

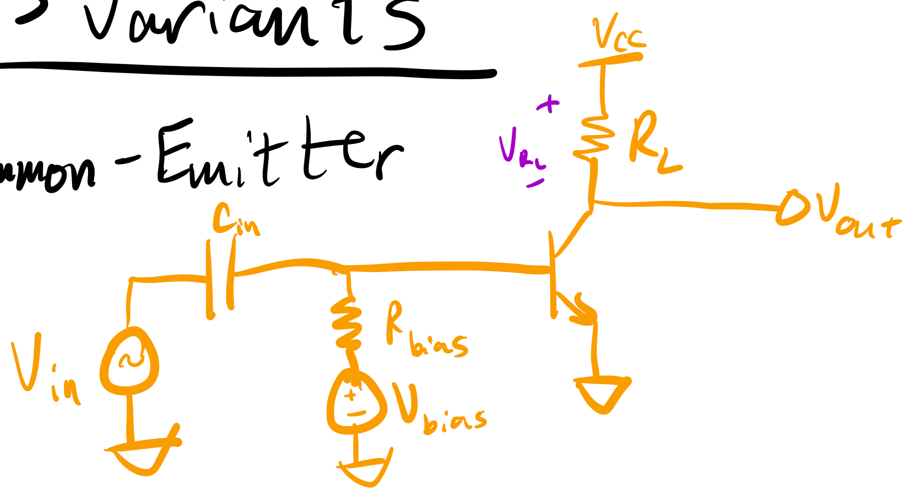
Potential further topics (based on interest and time):

- emitter degeneration
- single-BJT amplifiers
  - Common emitter, Common base, Emitter follower
- input and output resistance
- differential pairs
- parasitics and frequency response
- Common two-transistor amplifiers, and when to use them
  - Emitter follower → common emitter
  - Cascode
- current mirrors
- actively loaded amplifiers
- and much more!

Single-BJT Amplifiers

3 variants

- Common-Emitter



$$I_C = g_m V_{in}$$

$$V_{R_L} = I_{R_L} R_L$$

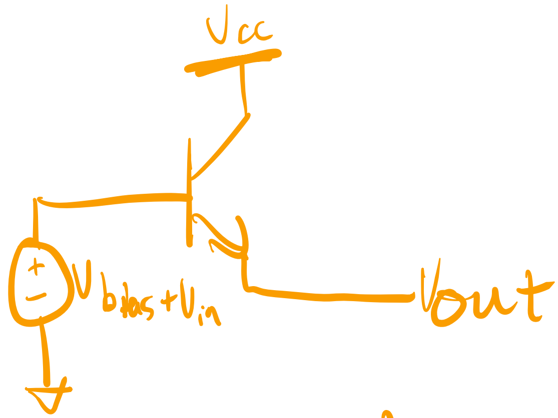
$$V_{R_L} = g_m V_{in} R_L$$

$$V_{out} = V_{CC} - V_{R_L}$$

$$= V_{CC} - g_m V_{in} R_L$$

$$\frac{dV_{out}}{dV_{in}} = -g_m R_L$$

- Emitter Follower (common collector)



Voltage buffer

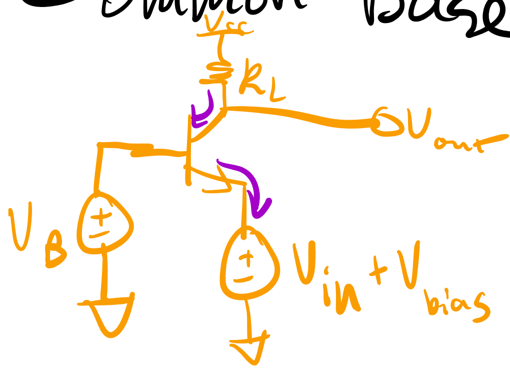
$a_v = 1$

assume I_C is mostly fixed

→ $V_{BE} \approx$ constant

→ $V_{out} = V_{bias} + V_{in} - V_{BE}$ $\quad \frac{\partial V_{out}}{\partial V_{in}} \approx 1$

- Common-Base



current buffer